ABSTRACT OF THE DISCLOSURE

A multiplexed address and data bus are provided for transferring data between two microprocessors. The multiplexed address and data bus include a plurality of multiplexed lines for communicating between the two microprocessors. A read/write signal line is also provided for communicating between the two microprocessors for indicating whether a read or a write operation is to be performed. A chip select line is provided for transitioning to an enable condition during a data transfer cycle. A data strobe line is in communication between the two microprocessors and provides a strobe signal for each sequence of a data transfer cycle.